

# **EMBEDDED MULTIPROCESSOR TECHNOLOGY FOR VHSIC INSERTION**

**Presented at  
Technology for Space Station Evolution  
- A Workshop**

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**Paul J. Hayes  
NASA Langley Research Center  
(804) 864-1491**

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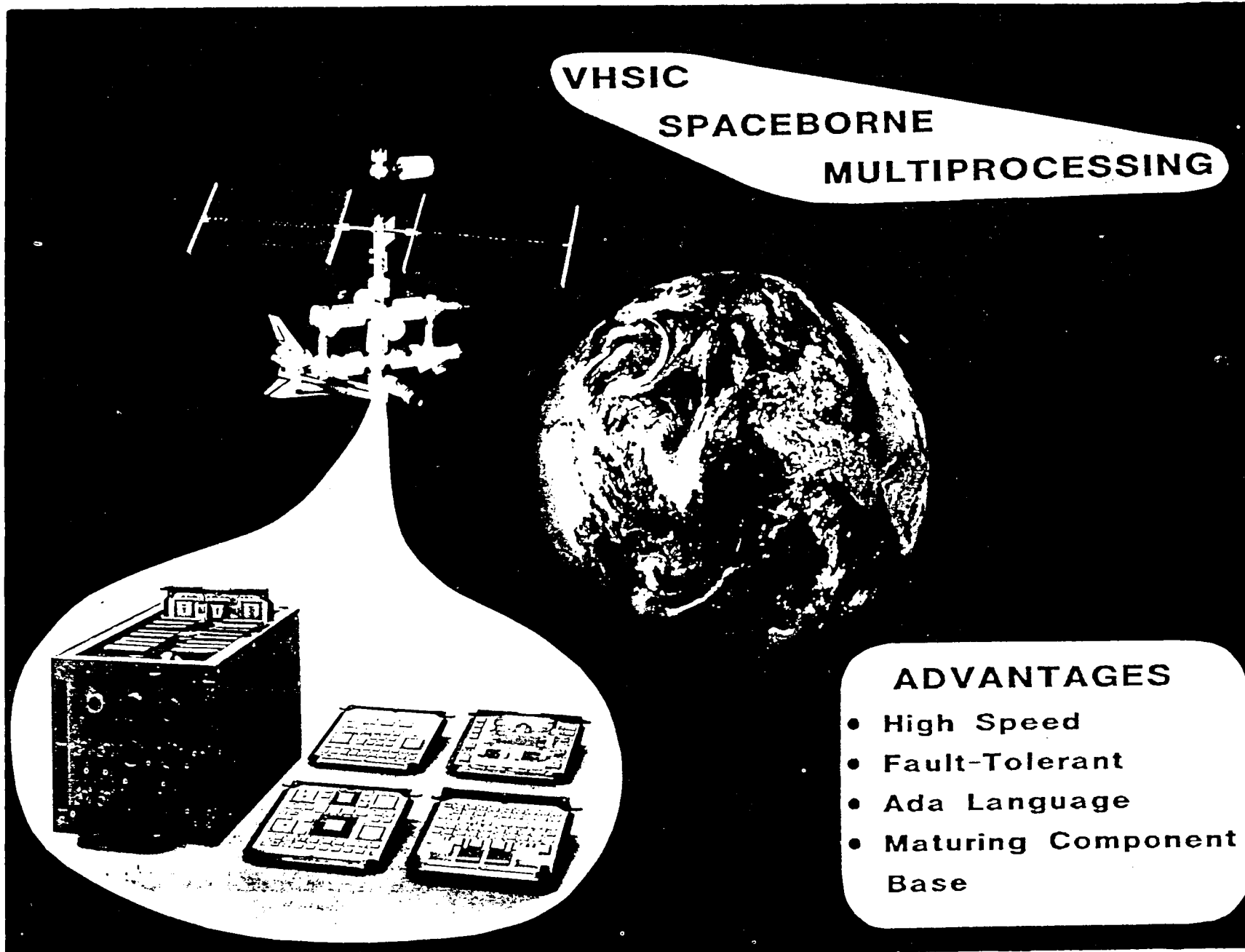
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**VHSIC  
SPACEBORNE  
MULTIPROCESSING**



**ADVANTAGES**

- High Speed
- Fault-Tolerant
- Ada Language
- Maturing Component Base

# **NASA MULTIPROCESSOR TECHNOLOGY**

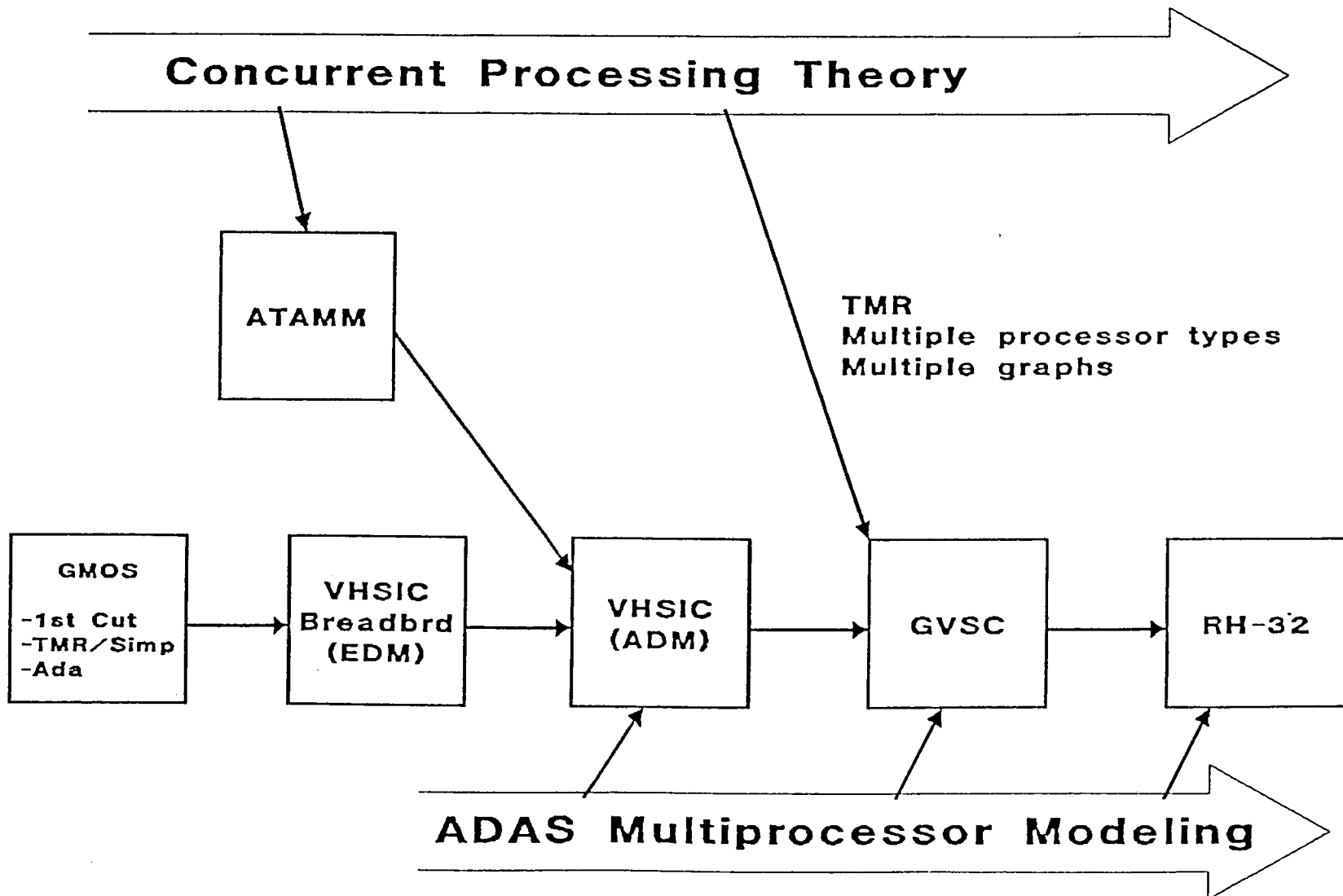
## **OBJECTIVE**

**Develop multiprocessor system technology providing user-selectable fault tolerance, increased throughput, and ease of application representation for concurrent operation.**

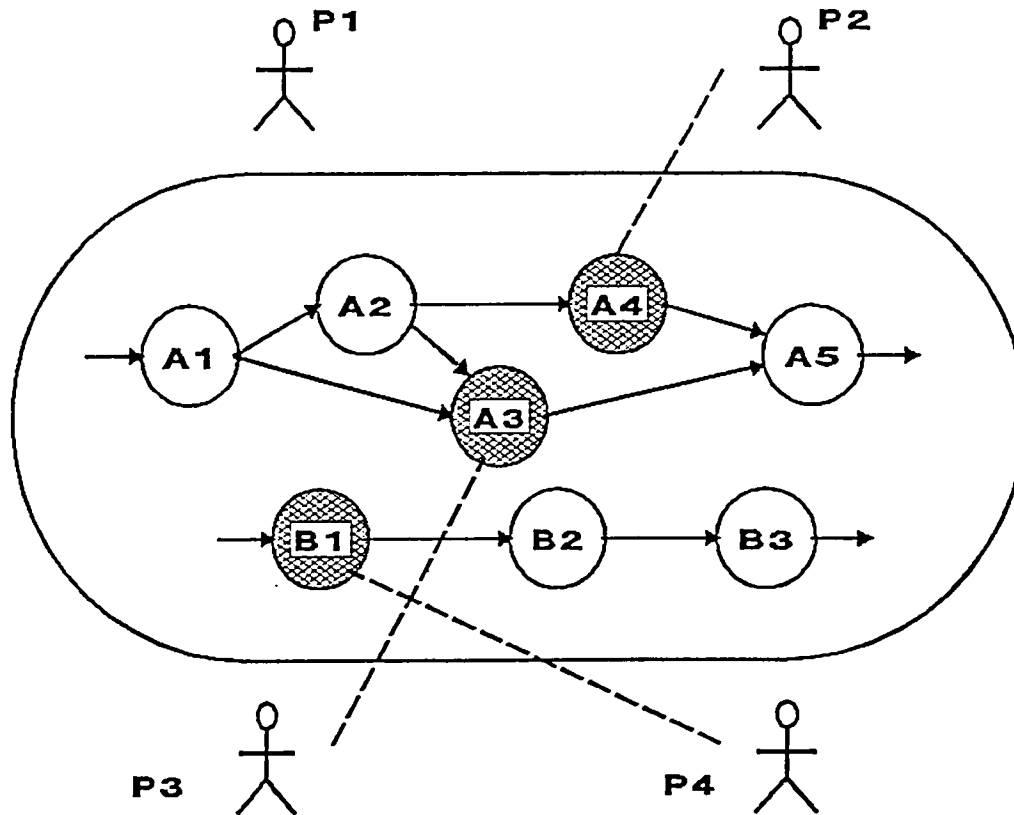
## **APPROACH**

**Develop graph management mapping theory for proper performance, model multiprocessor performance, and demonstrate performance in selected hardware systems.**

# MULTIPROCESSING TECHNOLOGY



# Graph Management Operating System (GMOS)



**Processor Assignment  
for Node Execution**

## Features

- Distributed O/S and Nodes
- Real-Time Node Assignment
- Application Graph
- Node-Selectable Fault Tolerance
- Ada
- VHSIC 1750A

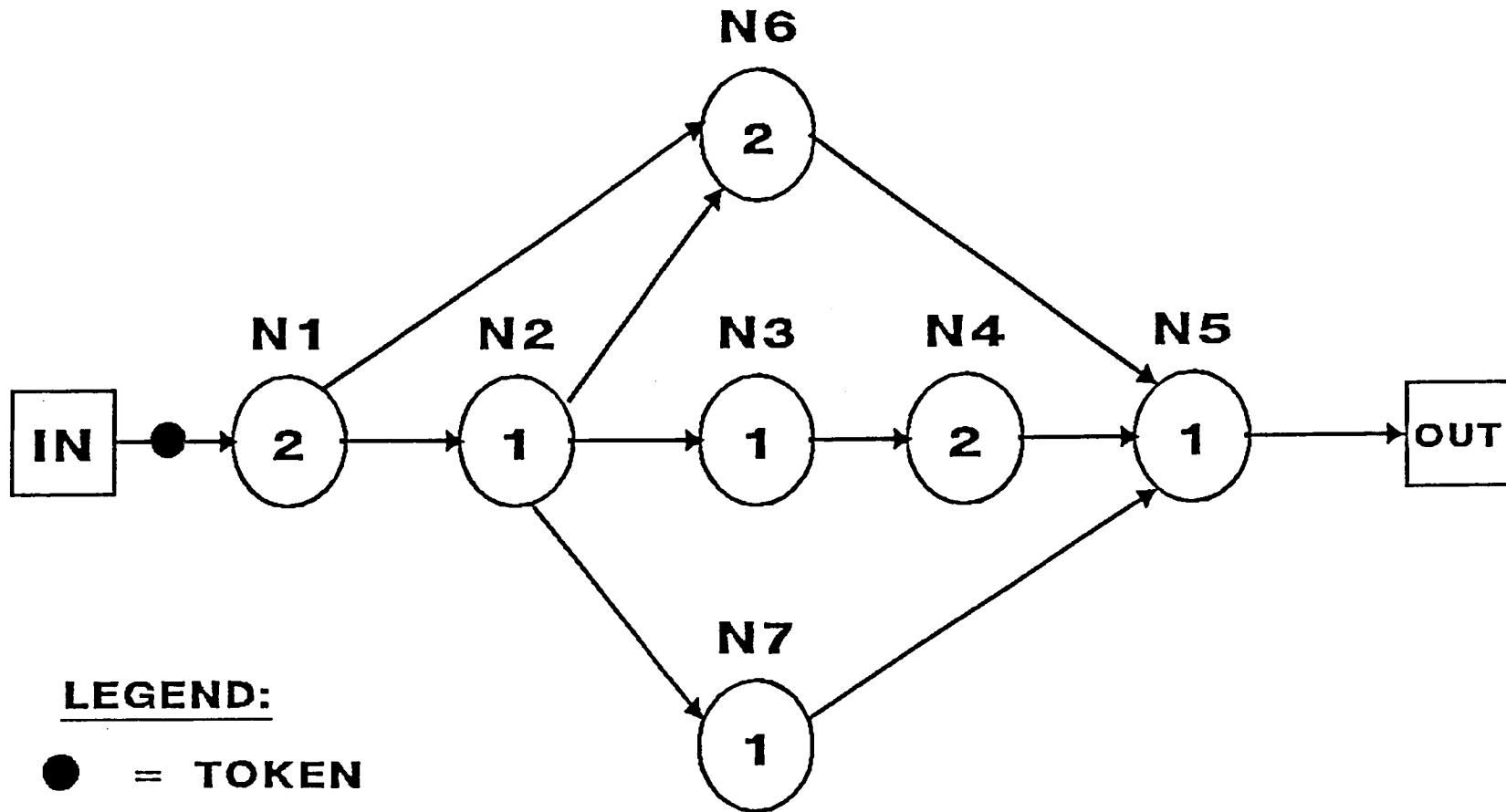
# **GMOS FUNCTIONAL FEATURES**

- **EXECUTES DIRECTED GRAPH - SINGLE GRAPH  
- MULTIPLE GRAPH**
- **GRAPH NODE CRITICALITY - TMR OR SIMPLEX**
- **GRAPH NODE SCHEDULING**
  - A) DATA DRIVEN - EVENT FLAG  
- SEMAPHORE (MULTIPLE EVENTS)  
- AND/OR LOGIC**
  - B) DEMAND DRIVEN - PERIODIC TIMER  
- ONE-SHOT TIMER**
- **BACKUP NODE ALLOCATION**
- **FAULTY PROCESSOR EXCLUSION, SELF TEST, REBOOT**

## **ALGORITHM TO ARCHITECTURE MAPPING MODEL (ATAMM)**

- **A strategy for the real-time assignment of the nodes of a data-driven algorithm graph to parallel processors**
- **Based on Petri-Net marked graph theory**
- **Aimed at large-grain graph applications**
- **Provides:**
  - **deadlock-free performance**
  - **optimum time performance**
  - **operating system rules**
  - **performance prediction**

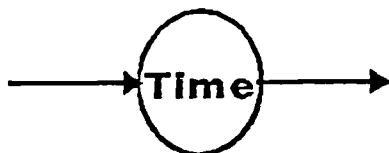
# ALGORITHM MARKED GRAPH (AMG) FOR 7-NODE EXAMPLE GRAPH



## LEGEND:

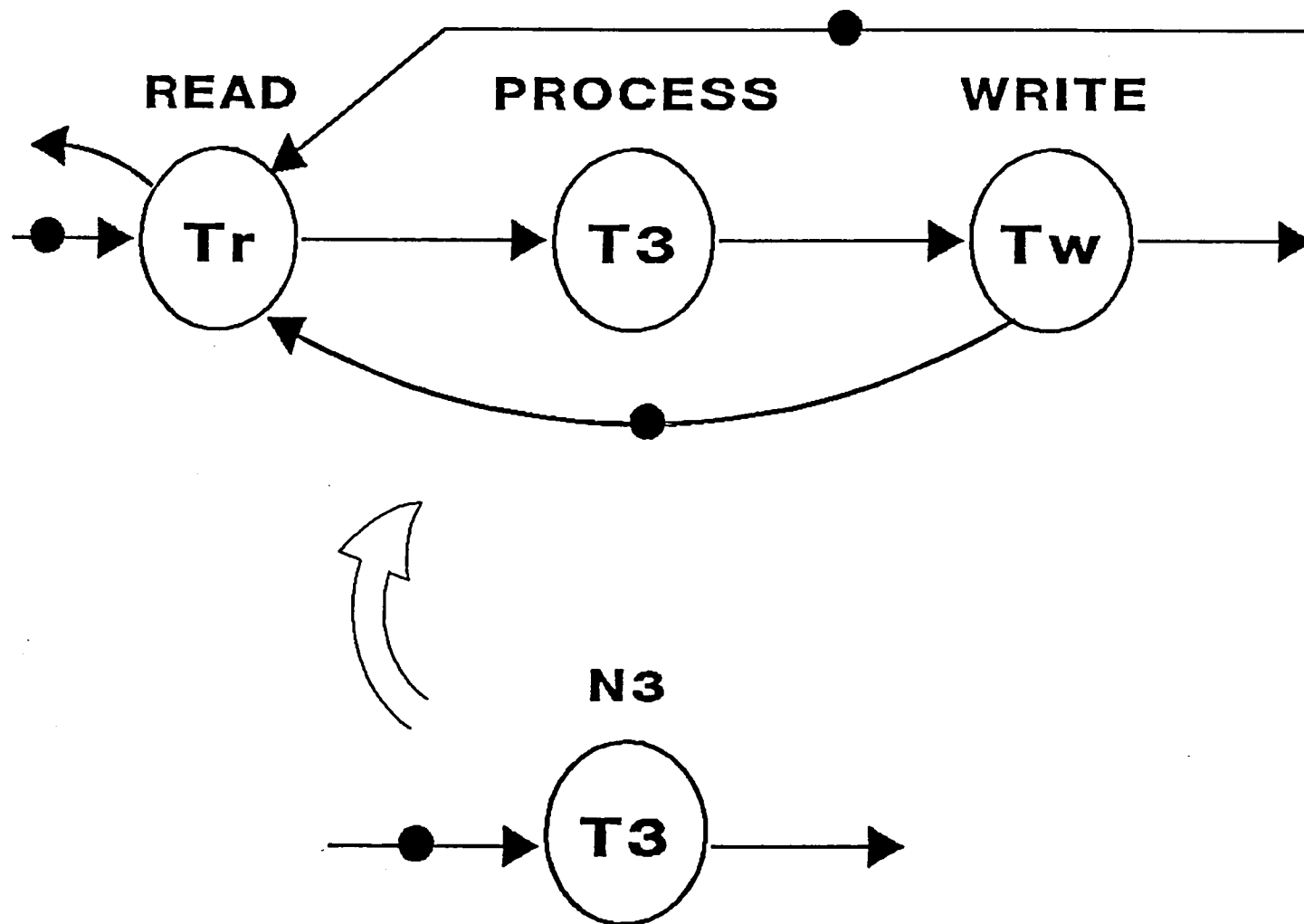
● = TOKEN

**Name**

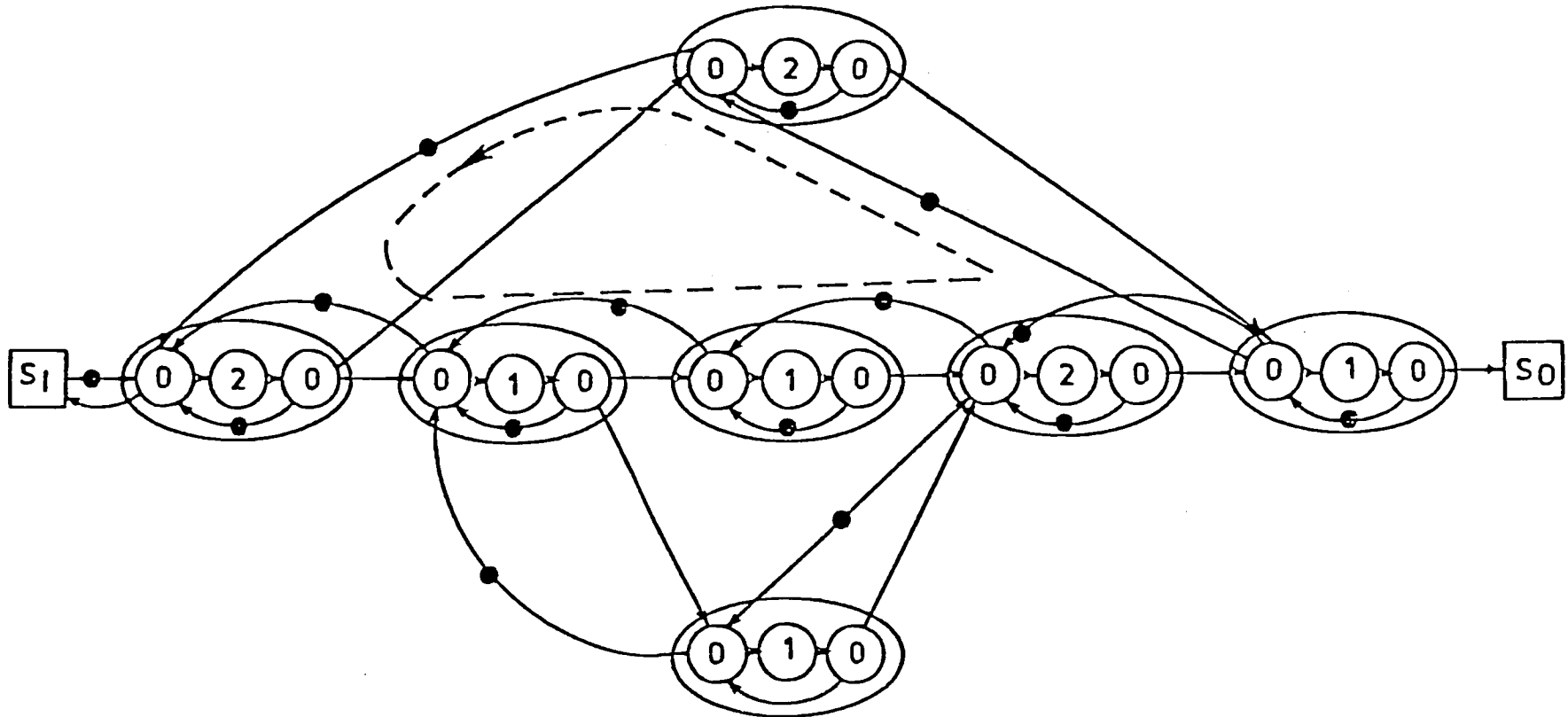




## NODE MARKED GRAPH (NMG) FOR DATA HANDLING



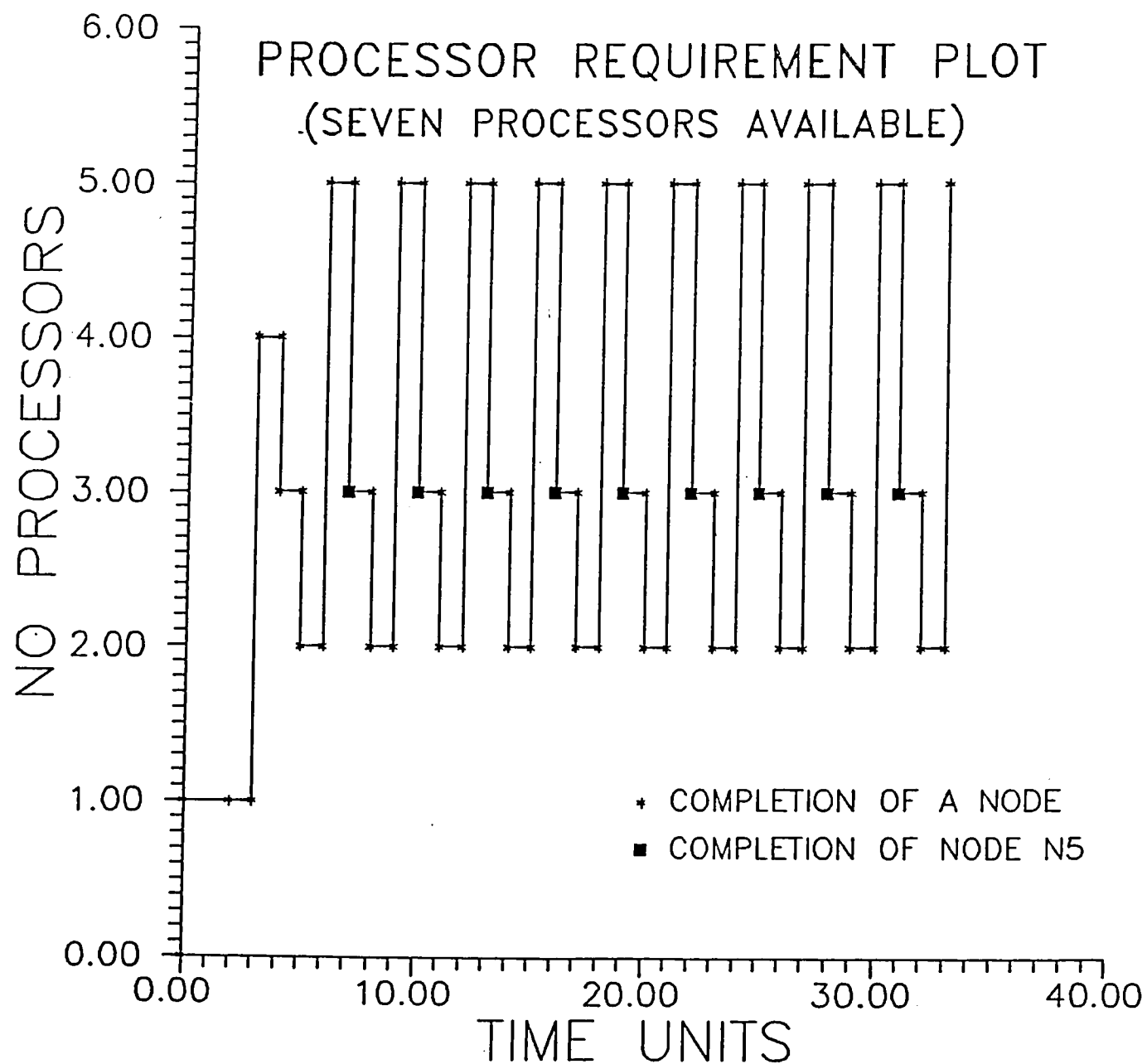
# GRAPH FOR ANALYSIS



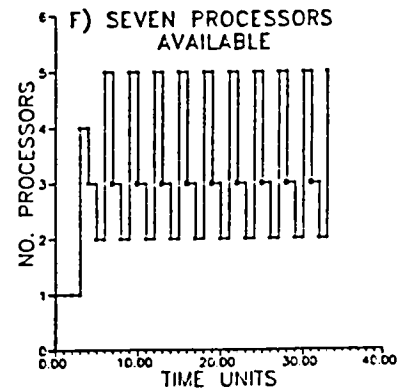
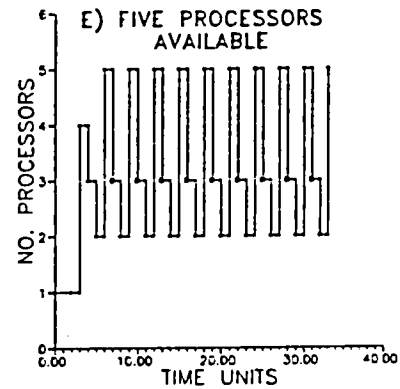
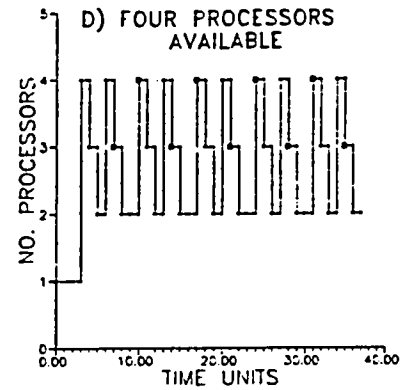
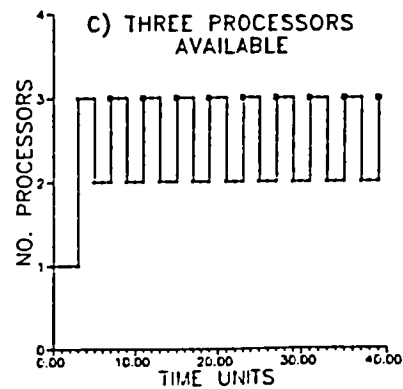
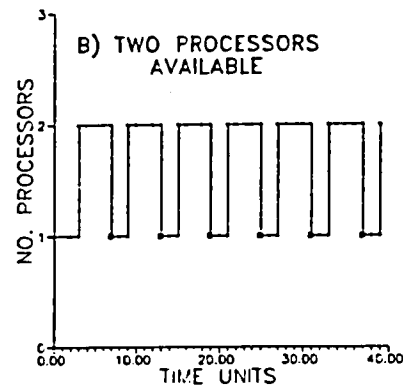
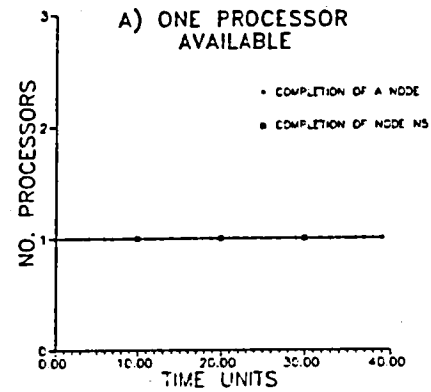
TBO = TIME BETWEEN SUCCESSIVE OUTPUTS

$TBO_M$  = MINIMUM VALUE FOR TBO

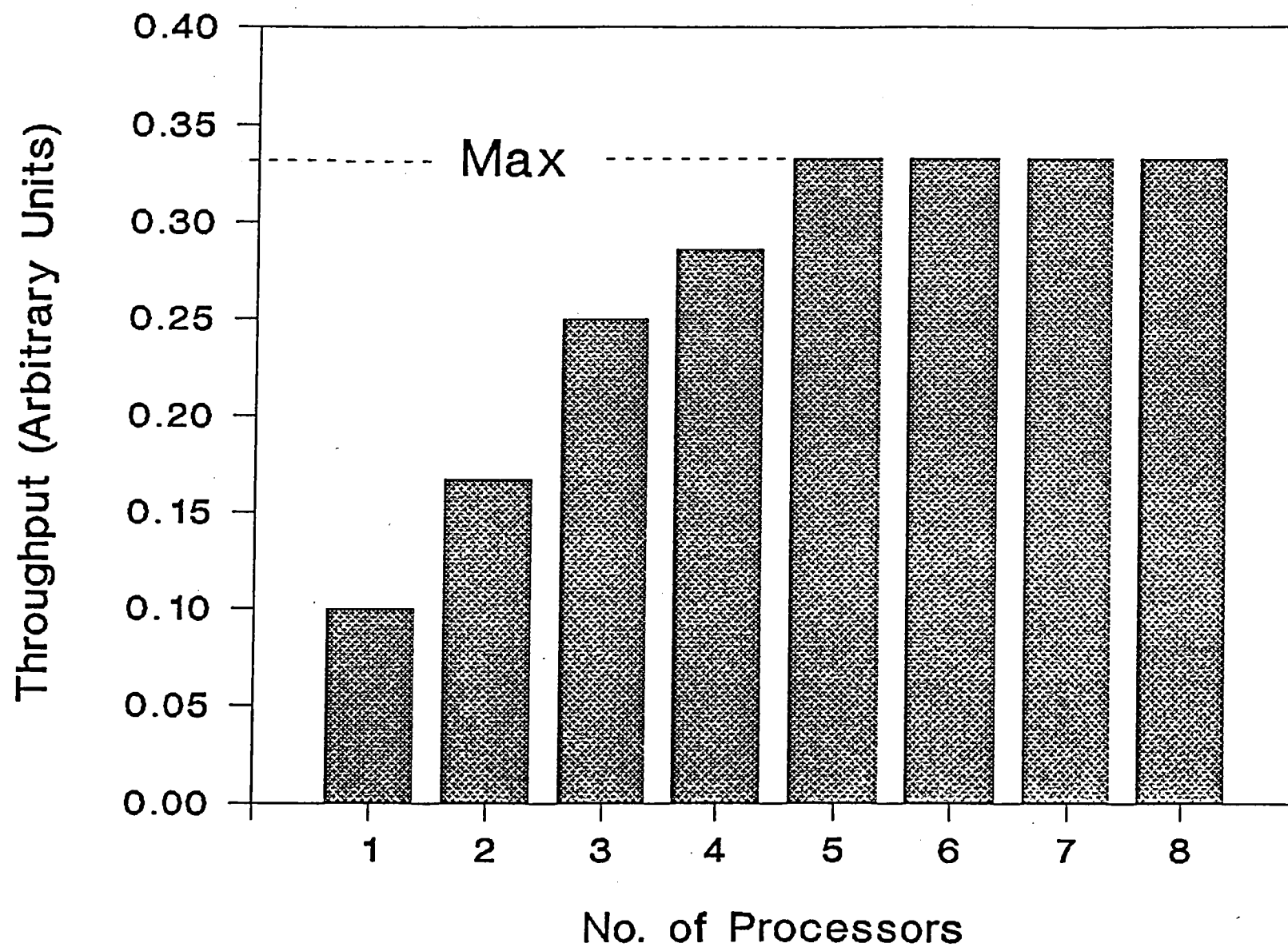
$$= \text{MAX} (\text{TIME/NO. TOKENS})_i = 6/2 = 3$$



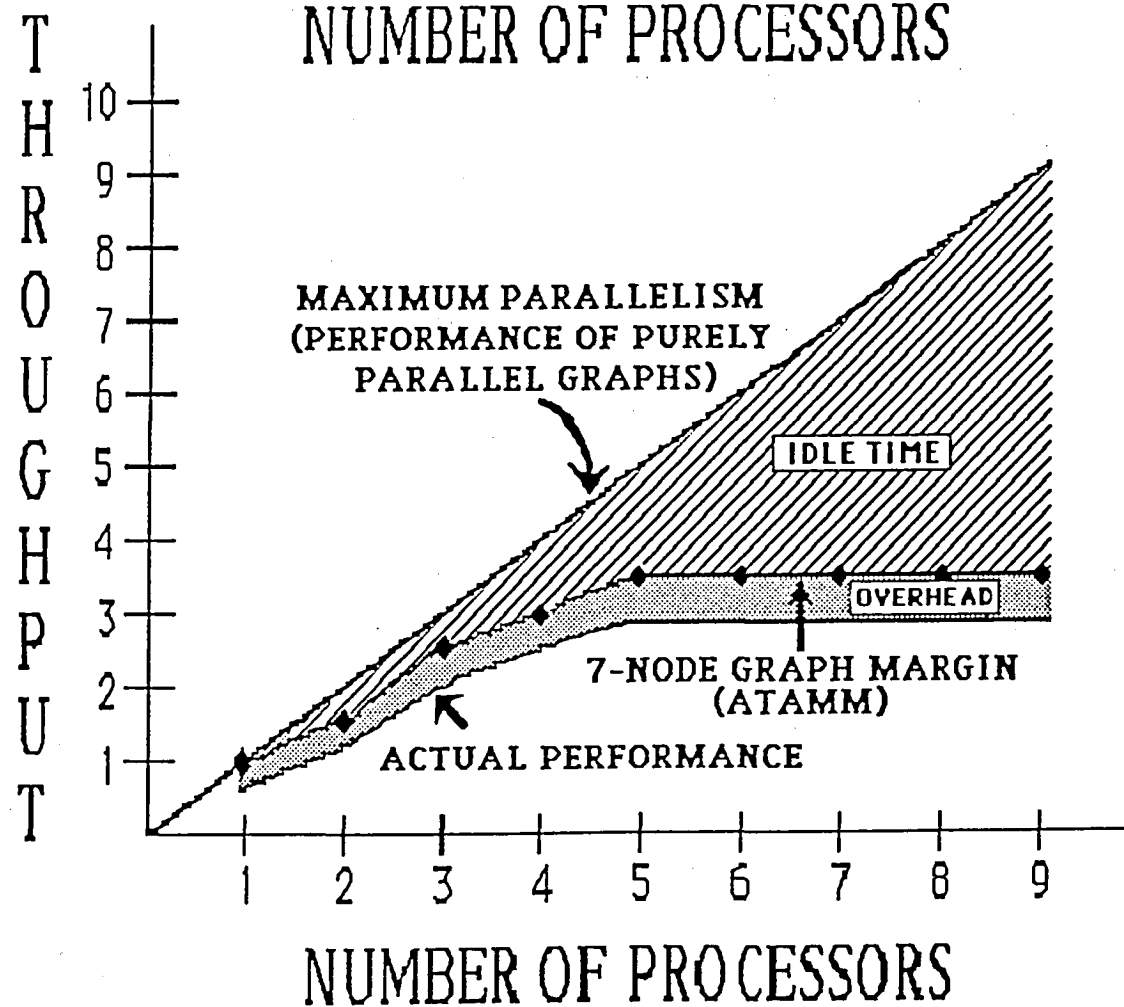
# PROCESSOR REQUIREMENT PLOTS



# PERFORMANCE MARGIN



# NORMALIZED THROUGHPUT VERSUS NUMBER OF PROCESSORS



## **ATAMM PROVIDES A NEW CAPABILITY SET**

- o Mathematically proven lock-free performance**
- o Operating system rules to manage the  
assignment of graph nodes to processors**
- o Prediction of graph's performance bounds**
  - Maximum data rate**
  - Maximum number of processors**
  - Dependency of data rate on number  
of processors**

# ATAMM DEVELOPMENT/DEMO PLANS

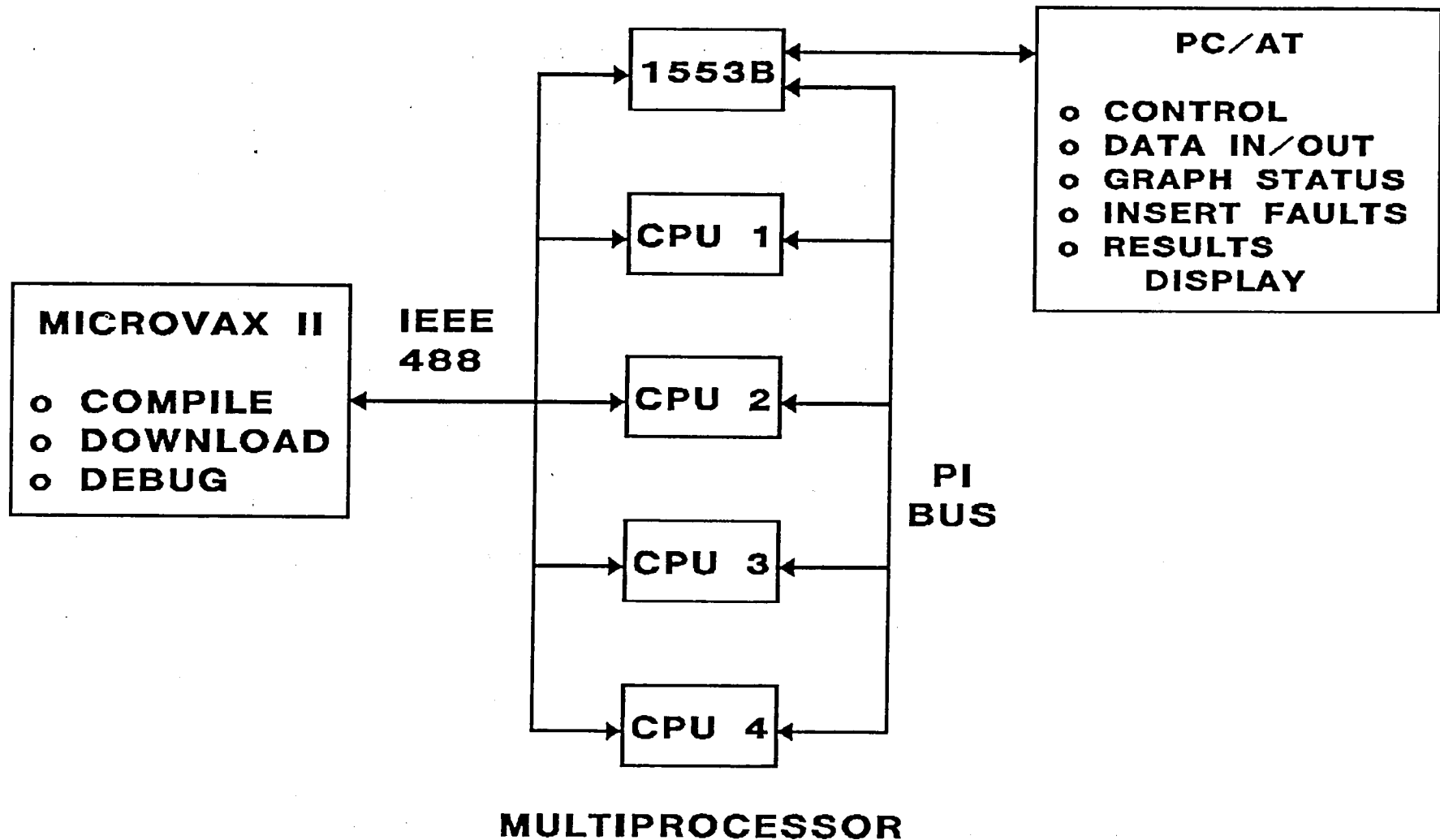
STATUS	FEATURE	DEMO
Initial ATAMM	<ul style="list-style-type: none"> <li>o Single graphs</li> <li>o Simplex</li> <li>o Identical processors (HW &amp; SW)</li> </ul>	ADM
Current Update	<ul style="list-style-type: none"> <li>o Triple Modular Redundant (TMR)</li> <li>o Graph optimization for specific no. processors</li> </ul>	
Future Features	<ul style="list-style-type: none"> <li>o Multiple graphs</li> <li>o Multiple iterations of the same graph</li> <li>o Multiple processor types</li> <li>o Variable node-latency times</li> </ul>	GVSC and/or RH-32



## **MAJOR RESEARCH THRUST FOR FY90**

- o Implement ATAMM Rules into KOS**
  - Simpler operating system than previous GMOS**
  - Use Westinghouse Directed Graph Tool**
  - Use 1553B to provide data I/O and monitor graph status**
  - Improved version of Ada compiler**
  - 2.5 MIPS VHSIC ADM 1750A processor**
  
- o Demo/Evaluate with Ada Algorithms**
  - Test Algorithm (Scan-to-scan track correlation for SDIO)**
  - Time-simulated graphs**
  - Simplex/TMR**
  - Fault injection and continued processing**

# MULTIPROCESSOR INTERFACE DIAGRAM





- **1.25 $\mu$  CMOS VHSIC**
- **$\mu$ -Coded CPU Plus 256K RAM**
- **Surface-Mounted Devices; Dual Board Module**
- **5.88 x 6.44 Inches (SEM-E)**

# MAJOR PROGRAM MILESTONES

	FY
1) Integrate/Demo ATAMM and SDIO Algorithm on Avionics Advanced Development Model (ADM)	90
2) Adapt/Demo ATAMM-Based OS on GVSC	91
3) Expand ATAMM Capability and Adapt/Demo on RH-32	94